contact area for the well 11. The gated diode is solely provided on the right-hand end and comprises the insulated gate 18 and the highly doped n-type zone 17 which partly overlaps the well 11. In this example, the gated diode is also arranged as a MOS transistor having a further n-type zone 19. The cathode of the SCR, formed by the highly doped n-type zone 14 is provided along the part of the periphery of the well 11 that is free from the gate 18 at a minor distance from the anode 8. The ratio between the two parts of the periphery may be chosen with relatively large freedom depending on the circumstances. Fig. 4 shows an embodiment in which the gated diode takes up only a relatively small part of the periphery of the SCR and thus has very little influence on the holding voltage V_h and on the current-conveying power of the SCR. At the position of the contact 20, the gate 18 is connected to the p-type substrate 10 and to the n-type cathode 14 which, together with the further zone 19, forms a coherent area. Needless to observe that, if so desired, the gate may also be connected to a junction in the circuit to another, suitable, voltage.

In the Claims

Please amend claims 1-3 and 7-9 as follows. A separate markup sheet accompanies this amendment.

1. (Thrice Amended) A semiconductor device having a semiconductor body which on a surface comprises an integrated circuit containing protection means for protection against electrostatic discharge (ESD), the means being a compound element of an SCR and a gated diode, the

protection means being provided in a surface area of a first conductivity type having a single well of a second, opposite, conductivity type,

wherein a surface zone of the first conductivity type forms a first anode and cathode area of the SCR element,

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the surface area has a surface zone of the second conductivity type, further denoted as first zone, situated remote from the well and forming a second anode and cathode area of the SCR element, and

the gated diode contains a gate insulated from the surface of the semiconductor body and a highly-doped second conductivity type surface zone aligned to this gate further denoted as second zone, which aligned surface zone partly overlaps the well of the second conductivity type, characterized in that the said second zone stretches out only along a part of the periphery of the well, the first zone is provided along at least another part of this periphery of the well which is free from the said second zone, and an anode and cathode of the SCR element in the first zone are not shielded from one another by the gated diode.

2. (Twice Amended) A semiconductor device as claimed in claim 1, characterized in that the gate of the gated diode substantially stretches out only along that part of the periphery of the well along which also the said second zone of the second conductivity type stretches out.

3. (Twice Amended) A semiconductor device as claimed in claim 2, characterized in that the gated diode is arranged in the form of a MOS transistor which has a further surface zone of the second conductivity type, deposited in the surface area of the first conductivity type, the said